01-14-00

A

jc490 U.S. PTO 01/14/00

jc525 U.S. PTO 09/482332 01/14/00

NON-PROVISIONAL APPLICATION FOR U. S. PATENT UNDER 37 CFR 1.53(b) TRANSMITTAL FORM

Attorney Docket No. TI-28063

Assistant Commissioner for Patents
Washington, D. C. 20231

"EXPRESS MAILING" Mailing Label No. **EJ134890768US.** Date of Deposit: **January 13, 2000.** I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 CFR 1.10 on the date shown above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Nancy Thornton

Sir:

Transmitted herewith for filing is the patent application of:

Inventor(s): Michael A. Lamson
Subhenu Kundu
Ramani Ramesh

For: **SYSTEM FOR ELECTRICALLY MODELING AN ELECTRONIC STRUCTURE AND METHOD OF OPERATION**

Enclosed are:

5 Sheets of formal drawings and 31 pages of Specification (including Abstract)
x A Declaration/Power of Attorney
x Assignment with form PTO 1595

Please amend the specification by inserting before the first line the sentence:
This application claims priority under 35 USC § 119 based upon **Provisional Patent Application number 60/116,274, filed 01/19/99.**

FEE CALCULATION					FEE
	NUMBER		NUMBER EXTRA	RATE	BASIC FEE $ 760.00
Total Claims	31	-20 =	11	X $22 =	$242.00
Independent Claims	3	- 3 =	0	X $82 =	$ .00
				Total Filing Fee	$1,002.00

Please charge **Deposit Account No. 20-0668** in the amount of the Total Fees set forth. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-0668. **This form is submitted in triplicate.**

All correspondence related to this application may be addressed to the undersigned at Navarro IP Law Group, P.C. 801 E. Campbell Rd. Suite 655, Richardson, TX 75081.

Date: January 13, 2000

Gary C. Honeycutt
Registration No. 20,250

01-14-00 A

Navarro IP Law Group, P.C.

Specializing in Patents, Trademarks, Copyrights and other Intellectual Property Matters

A Professional Corporation
801 E. Campbell Road
Suite 655
Richardson, Texas 75081

(972) 238-7160 - Tel
(972) 238-7013 - Fax
honeycutt@kniplaw.com

January 13, 2000

VIA EXPRESS MAIL NO. EJ134890768US

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Patent Application For:
SYSTEM FOR ELECTRICALLY MODELING AN ELECTRONIC STRUCTURE AND METHOD OF OPERATION
Attorney Docket No. TI-28063
Our File: 1000-2056

Dear Sir:

Enclosed for filing please find the following items relating to the above-identified application:

(1) Non-Provisional Application;

(2) Fee Authorization/transmittal Form ;

(3) Declaration, and Power of Attorney;

(4) Assignment and Recordation Form Cover Sheet

(5) Specifications and Formal Drawings; and

(6) Postcards.

Please charge **Deposit Account No. 20-0668** in the amount of the total fees set forth. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to **Deposit Account No. 20-0668.**

Please file the application and return the date-stamped postcard to the corresponding addresses as indicated. In the meantime, if you have any questions or comments concerning this matter, please call the undersigned. Otherwise, please accept the enclosed.

Sincerely,

Gary C. Honeycutt
Reg. No. 20,250

GCH/ntn
Enclosure

SYSTEM FOR ELECTRICALLY MODELING AN ELECTRONIC STRUCTURE, AND METHOD OF OPERATION

FIELD OF THE INVENTION

The present invention is related in general to the field of electronic systems and semiconductor devices and more specifically to improved systems and methods for electrically modeling an electronic structure such as an integrated circuit package and assembly.

DESCRIPTION OF THE RELATED ART

Designers of semiconductor integrated circuits (ICs) have used modeling of electrical characteristics for a long time in order to arrive at optimized layouts for the ICs. One of the best known IC modeling systems is called SPICE ("Simulation Programs for Integrated Circuits in Electronics"). For the package, however, which encapsulates the IC no such modeling system exists. Packages are not fine-tuned to leave the IC characteristics undiminished; for example, loss of speed, frequency limitations, cross talk, noise are often observed.

These limitations have become intolerable for the increasing performance demands on ICs. The trends of leadership chips, to be matched by their prospective packages, call for 100 picoseconds edge rates, equivalent to more than 2.6 gigabit/second clocks; lead counts in excess of 1000; collapsing power rails at 1.8 volts, calling for lower noise budget; higher power dissipation, requiring higher capabilities for changing current in time; packages

less than 1 millimeter thick; tighter package lead pitch; and last but not least, lower cost.

It is that market trend listed last which is now becoming all-pervasive. As a consequence, the cycle time needed to design a new package is soon required to shrink to approximately 2 weeks; furthermore, it is becoming more and more mandatory to use mostly low cost materials and existing installed manufacturing machines. In addition, reliability expectations for the semiconductor device are increasing in order to lower the cost of ownership; designing-in and building-in reliability through optimized design and process control are the methods proposed to reach the improved product reliability.

In order to meet these often conflicting requirements and to support these ambitious trends, the electrical design of packages for IC devices must more and more be based on sensitive modeling and analysis. Guided by the Semiconductor Research Corporation (SRC), universities such as the University of Arizona at Tucson or the University of California at Berkeley, have been creating and developing electrical simulation and analysis programs for semiconductor packages for several years. While these calculation programs are accurate, their application turned out to be cumbersome in the practical world of industry designers, and sometimes unnecessarily detailed. Unfortunately, there is no system available in known technology which combines a straightforward application of the electrical programs developed at universities with user-friendly features of simplicity, flexibility, and time saving as required by the competitive reality of the semiconductor industry.

An urgent need has therefore arisen for a low-cost, fast and reliable system and a method of operation providing

electrical modeling and analysis of electronic structures. The system should provide the opportunity to model the electrical performance of complete semiconductor packages as well as individual parts of it, packages alone as well as in combination with the integrated circuit chip, and semiconductor devices assembled on boards. The system and method should be flexible enough to be applied for different semiconductor product families and a wide spectrum of design, material and process variations, and should spearhead the way for very high frequency, high power packages, as well as toward the goals of improved product yield and device reliability. Preferably, these innovations should be accomplished using conventional workstation and personal computers so that no investment in powerful computing equipment is needed.

SUMMARY OF THE INVENTION

According to the electrical modeling system and method provided by the present invention, the electronic structure to be modeled is segmented into an ordered sequence of sections, each section is electrically analyzed individually, and the resulting data is collated, or integrated back again to create the electrical model of the complete structure, whereby the model output is preferably created in a format generally suitable for electrical models of integrated circuits. Examples of electronic structures which can be modeled by the system and method of the invention include leadframes, packages, complete devices, and electronic devices assembled on motherboards.

The present invention is related to high density ICs, especially those to be used at very high frequencies and having high numbers of input/outputs and tight constraints in package outline and profile. These ICs can be found in many semiconductor device families such as processors, standard linear and logic products, digital and analog devices, high frequency and high power devices, and both large and small area chip categories. Since the invention aims at designing devices with minimum geometries and high reliability, it supports continually shrinking applications such as cellular communications, pagers, hard disk drives, laptop computers and medical instrumentation.

It is an object of the present invention to provide an automated system and method for electrically modeling an electronic structure. The object is achieved by an embodiment of the invention using a computer system and a

computer-implemented method for automatically analyzing and modeling the electronic structure.

Another object of the present invention is to provide a highly flexible system and method. This object is achieved by the embodiments of four subsystems of the invention:

* A user-friendly interface operable to accept user instructions and to control the system operations at a plurality of software control points.

* An input data generator operable to accept graphical and geometric inputs, to create patterns of electrical conductors and insulators, and to accept compositional and functional parameters.

* A model data analyzer operable to perform two-dimensional and three-dimensional analyses and mixtures thereof.

* A model output generator operable to create the model in a plurality of formats, especially those suitable to interface with electrical IC models.

Another object of the present invention is to provide an electrical model of an electronic structure in fast turn-around time and with minimum effort by taking full advantage of symmetries and branching of the structure. This object has been achieved by the embodiments of three subsystems of the invention:

* A segmentation generator operable to select segments of the structure to be modeled and to organize the sequence of these segments.

* An analysis generator operable to electrically analyze those segments in a plurality of calculation programs, executed in sequence.

* An integrator operable to collate and integrate the analysis results in controlled sequence into a single model.

Another object of the present invention is to introduce modeling concepts which are flexible so that they can be applied to many families of electronic structures -- reaching from piece parts, such as leadframes, to device packages, to complete semiconductor IC products, to electronic substrates, and to whole assemblies on motherboards -- and are general so that they can be applied to several generations of products.

These objects have been achieved by teachings and embodiments of the invention. Various modifications have been successfully employed to satisfy different selections of product geometries, compositions and characteristics. The method of the invention provides easy expansion to new fields of IC modeling, such as inclusion of three-dimensional contributions, or transmission and shielding effects in ultra-high frequency products. Further, the method of the invention provides easy specialization to customer-specific requirements, such as ranking of the options for minimizing certain product parameters.

The technical advances represented by the invention, as well as the objects thereof, will become apparent from the following description of the preferred embodiments of the invention, when considered in conjunction with the accompanying drawings and the novel features set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a block diagram of a system for electrically modeling an electronic structure according to the invention.

FIG. 2 illustrates a block diagram of a computer system for electrically modeling an electronic structure including a first embodiment of the present invention.

FIG. 3 illustrates a block diagram of the detail of the input data generator and the input data storage according to the invention.

FIG. 4 is a flow chart of the method used to generate inputs in the format suitable for the model analysis, including a second embodiment of the invention.

FIG. 5 is a flow chart of the method used in the model data integrator to generate model outputs, including a third embodiment of the invention.

FIG. 6 is a flow chart of the method used by the user interface to control the modeling operations, including a fourth embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

One major problem associated with electrical analysis and modeling of an electronic structure, such as an integrated circuit (IC) package, is the time it takes to complete the analysis after all the elements have been generated. This is true even for piece parts of an IC package, such as a metallic leadframe. One way of avoiding some of this processing time is to exploit features of symmetry and branching found in the electronic structure in order to cut down the number of elements that must be processed. However, due to the complex geometries and compositions found in most electronic structures, such as contemporary packages, the definition of the most effective segmentation of the structure emerges as a pivotal ingredient of successful electrical modeling.

A second problem with electrical analysis and modeling of an electronic structure is the flexibility to put the model parts automatically together again such that they provide not only the model of the complete structure, but also quantify alternative choices to the user. With this capability, existing limitations and potential variations of the electronic structure can be highlighted -- major ingredients of reliability insurance and innovative solutions.

A third problem is the wide variety of inputs generally presented to the model generator. An automatic standardization and input format definition simplifies the job of effective analysis in short turn-around time.

As illustrated schematically in the simplified block diagram of FIG. 1, the system of the present invention,

generally designated 100, operates to automatically provide segmentation as well as integration for creating an electrical model of an electronic structure. An input data generator 110 generates input data which describe a variety of characteristics of the structure to be modeled. Included in these characteristics are geometries, graphics and data related to any segments, subdivisions, materials, and other parameters. Input data generator 110 is connected to a segmentation generator 120 which selects the segments of the structure to be analyzed. It further organizes the correct sequence of these segments, and then stores the data related to the segments, arranged in sequence, in a segment file. Afterwards, the data of this segment file is converted into a format suitable for electrical analysis.

The segmentation generator 120 is connected to the analysis generator 130 which electrically analyzes the converted data of the segment file in a multitude of calculation programs. These programs are automatically executed in sequence, and the results of the electrical analysis are stored in an analysis output file.

Coupled to the analysis generator 130 is an integrator 140 which integrates the analysis output into a single model. This integration is performed in an automatically controlled sequence, and the model is filed in a report storage. From this storage, an output generator 150, coupled to the integrator 140, creates the summary files in a plurality of predetermined formats, or displays the model results on a display monitor.

Modeling system 100 can be used to model and analyze electronic structures such as a metallic leadframe, as used in electronic devices; a complete IC package; an IC package with an IC chip assembled inside; a substrate with conductive patterns embedded in an insulating medium, as

used for electronic devices; any pattern comprising electrical resistances, capacitances, and inductances; or a semiconductor device assembled on an electronic substrate. An embodiment of the present invention may be embedded in an IC; another preferred embodiment is a computer system.

For an embodiment in a computer system, examples of the requirements are as follows:

** Hardware:

* Platform/ Model	SUN SPARC station, such as 4/60, 4/65, 4/75 HP 9000 Series 700, such as 710, 720
* Memory	32 Mbytes
* Disk	100 Mbytes minimum
* Peripherals	None

** Software:

* Operating System	SOLARIS 2.5 and above HP 9000 Series 700, such as HP-UX 9.X Any X Window™ Manager
Other Software	Pro/ENGINEER™ X11R5
* Technology	Independent
* Input	IGES ("Initial Graphics Exchange Specification") DXF ("Drawing Exchange Format")
* Output	SPICE ("Simulation Program with Integrated Circuit Emphasis") for use with IC designs IBIS ("I/O Buffer Interface Specification") for use with system designs Summary file (electrical parameters for each frequency) Report file (lumped values of electrical parameters for all leads, variation of parameters with frequency

		S-Parameter files ("scattering parameters")
*	Other Interfaces	AutoCAD™ ("Automatic Computer Aided Design")
		SPICE
		EESOF

Pro/ENGINEER ™ is produced by Parametric Technology Corporation, Waltham, MA, USA. AutoCAD™ is produced by Autocheck Incorporated, Cupertino, CA, USA.

An embodiment of the computer system of the present invention is illustrated in the schematic block diagram of FIG. 2 and generally designated 200. The major parts of the computer system are, analogous to FIG. 1, the input data generator 210, the segmentation generator 220, the analysis generator 230, the integrator 240, and the output generator 250.

The input data generator 210 accepts and stores graphical, geometric, functional and compositional inputs; it further is able to create patterns of electrical conductors and insulators of a structure to be modeled. Data input generator 210 is described in more detail in conjunction with FIG. 3.

Coupled to input data generator 210 in FIG. 2 is a segment selector 221. It selects the segments and test lines of the structure to be modeled; it further selects the input data correlated to the segments and test lines from the input data generator. This data is then stored in the input data storage 222 (described in more detail in FIG. 3).

The segment selector 221 exploits any symmetry and branching exhibited by the structure to be modeled. By way of example, structures such as leadframes or packages may be symmetrical to only one axis; in this case, one needs to model only half of the leadframe or package; the results for the other half are reflected as required to get the complete

model. Analogous considerations hold for two or more symmetry axes.

Input data storage 222 of FIG. 2 is connected to sequence organizer 223, which arranges the selected segments in the correct order for modeling. The sequence organizer 223 further creates the segment data files stored in the segment data storage 224. Input data storage 222 is further connected to a user interface 260. This user interface 260 responds to user commands for controlling the execution and timing of a multitude of operations of the computer system. A major part of the user system is the operations controller 261 which provides automated control functions at a plurality of points in the modeling process flow (described in more detail in conjunction with FIG. 6).

Sequence organizer 223 in FIG. 2 is further connected to the parameter data storage 270. This data storage contains parametric data on all analysis types, standard values for materials properties, and can specify global parameters applicable to the electronic structure to be modeled. Parameter storage 270 can be supplied with data from the user interface 260, with which it is coupled.

A key embodiment of the present invention is model data translator 225. It is coupled to segment data storage 224 and reads the segment data files stored there. Translator 225 is also coupled to the operations controller 261 embedded in the user interface 260; it can thus follow instructions from controller 261. Model data translator 225 converts the segment data into a format suitable for electrical analysis by any computational program used in the model data analysis. The results of this conversion are stored in the analysis input storage 226.

The analysis generator 230 in FIG. 2 is the actual analysis engine of the modeling system. It contains the

model data analysis 231 which is coupled to the analysis input storage 226 and further to the operations controller 261 embedded in the user interface 260. The model data analysis 231 executes a plurality of electrical calculation programs in sequence, and creates the electrical analysis output files which are stored in the analysis output storage 232.

In the preferred embodiment of the invention, the electrical calculation programs used by the model data analysis 231 are typically invoked multiple times during an analysis run to cover all test lines and specified frequencies. Most of these programs have been developed by the University of Arizona at Tucson; they include two-dimensional electrical analysis programs and three-dimensional electrical analysis programs for capacitance as well as inductance calculations (including bends, steps, and vias). The analysis output files 232 contain capacitance, inductance and resistance per centimeter of conductor length in matrix format.

The format of the output may be such that in the capacitance matrices, the diagonal entries describe the self-capacitance of the conductor, while the off-diagonal entries describe the coupling capacitance between two conductors. In the inductance matrices, the diagonal entries describe the self-inductance of the conductor, while the off-diagonal entries describe the mutual inductance between two conductors. In the resistance matrices, the diagonal entries describe the resistance of the conductor. When modeling with symmetry, the cross coupling effect of conductors beyond any symmetry axis is calculated by adding extra conductors as needed whenever possible.

The integrator 240 in FIG. 2 includes the model data integrator 241 which is coupled to the analysis output

storage 232 and further to the operations controller 261. The model data integrator 241 integrates the analysis output files in 232 in controlled sequence into a single model file stores this model file in the report storage 242.

This report storage 242 is connected to the output generator 250, which is further coupled to the user interface 260. The output generator 250 creates the electrical model for each frequency analysis in the desired format. Examples of preferred output formats include SPICE-acceptable decks, IBIS decks, S-Parameter files, summary reports, and generally displays on monitors.

FIG. 3 illustrates, in a schematic block diagram, the input data generator of the computerized modeling system in a preferred embodiment of the present invention. The input data generator 210 comprises a number of graphics inputs; shown are inputs from Pro/ENGINEER™ 311 and AutoCAD™ 312. The geometric or graphical program for Pro/ENGINEER™ has to be in the IGES format, the geometric and graphical program for AutoCAD™ in the DXF format. In either case, the system provides to accept, select, read and edit an existing drawing of the structure to be modeled, or to draw a structure from scratch. Usually, the structure will consist of patterns made of electrical conductors or insulators, or both.

In order to supply the compositional and functional parameters needed for quantitatively characterizing the input graphics, the input data generator 210 provides the parametric input unit 313. It is also coupled to segment selector 221.

The segment selector 221 serves the pivotal function of defining subdivisions of the structure suitable for electrical analysis. A suitable subdivision, or section, consists of a set of continuous conductors. Any

discontinuity, such as a bend, marks the end of a subdivision. The system user can indicate a subdivision by drawing so-called "testlines" across the set of conductors in that subdivision. A testline should be at the center of the conductors and perpendicular to them. One can draw several testlines to cover all the subdivisions of the structure to be modeled. When a testline crosses a conductor, it has to cross both edges of the conductor.

In order to simplify the job of the sequence organizer 223 to establish the correct segment order for analysis, rules or conventions for the sequence of the testlines have to be established and followed. As an example, when the structure to be analyzed is a semiconductor package with a leadframe, the rule for ordering the testlines may be such that the conductor subdivisions they identify start from the chip side of the package to the outside.

In FIG. 3, the input data storage 222 is shown with a storage 321 reserved for files in the IGES format, and a storage 322 reserved for files in the DXF format. These are examples and preferred embodiments of the organization of input data storage 222; other examples and formats are possible. The input data storage is connected to both the sequence organizer 223 and the user interface 260 (see FIG. 2).

After creating the segments in segment selector 221, the segments are arranged in the correct order by segment organizer 223; the correct order is controlled by operations controller 261. The segment data, supplemented by parametric data from parameter data files 270, are filed in segment data storage 224. FIG. 4 details the flow diagram for the computer-implemented method how the model data translator 225 reads the segment data storage 224 (in IGES

or DXF format) and converts it to the input files required for electrical analysis (and stored in analysis input storage 226).

Referring to FIG. 4, the method of conversion begins in step 401 as the system is reading the first segment filed in the segment data storage. The system then identifies all element groups that form a segment by a series of automatic steps. Assuming first that the segment is of three-dimensional nature, the system determines in step 402 whether the end of the three-dimensional segment has been reached. In step 403, the system generally finds the edges of the geometry in the segment; in step 404, the system orders the edges in the correct sequence.

If the answer to check 402 is "yes", the system finds the edges of the three-dimensional geometry in step 403a, and orders the edges in the correct sequence in step 404a.

In step 407, the system converts the data of the ordered segment edges into the input format for electrical analysis. For the three-dimensional segment, after the ordering of the edges in step 404a, the system builds the input format for the ordered three-dimensional segment in step 407a. The system transfers the data converted into the analysis input format to the analysis input storage 226, which is connected to the model data analysis generator. In addition, the system uses the converted data from step 407a to determine in step 408 whether another segment is stored in segment data storage 224. If the answer is "yes", then the system repeats the process flow starting with reading the next segment in step 401. All process steps are repeated until all segments in segment data storage 224 have been read and converted. If the answer in checkpoint 408 is "no", the system proceeds to analysis input storage 226 coupled to the model data analysis generator.

If the answer to check 402 is "no", the end of the three-dimensional segment has not been reached; the system then finds the edges of that segment geometry in step 403b, and orders the edges in the correct sequence in step 404b.

In step 405, the system determines the segment is of two-dimensional geometry. If the answer is "no", the system stores the geometry of the segment in step 406 and forwards it to checkpoint 408 to determine whether another segment is stored in segment data storage 224. If the answer is "yes", the system builds the input format for the ordered two-dimensional segment in step 407b. The system transfer the data converted to the analysis input format to the analysis input storage 226, which is connected to the model data analysis generator. In addition, the system uses the converted data from step 407b to determine in step 408 whether another segment is stored in segment data storage 224.

FIG. 5 details the flow diagram for the computer-implemented method how the model data integrator 241, as part of the integrator 240, reads the analysis output storage 232 and integrates the analysis output files into a single model file. Referring to FIG. 5, the method of integration begins in step 501, as the system is reading the analysis output file recorded in the analysis output storage 232, as supplied by the model data analysis. The system then controls this analysis output by reading each segment (step 510) from the segment data storage 224 (as supplied by the sequence organizer) under the guidance of the operations control V (to be designated 650 in FIG. 6). As described in conjunction with FIG. 2, the overall operations controller 261, including operations control V, is imbedded in the user interface 260 and connected to the segment data storage 224 through the input data storage 222. The combination of

reading and controlling enables the collating of the sequence list (step 511) of the analysis output data, an important step of computer system embodiment of the present invention.

With the collated sequence list, the system determines electrical connectivity and branching in step 502. The analysis output data can thus be collated into electrical models of complete electronic structures (such as leadframes, packages, assemblies), from which the system creates the analysis output 503 in suitable format. As an example, FIG. 5 emphasizes SPICE decks, since SPICE format is conventionally used for IC designs. All analysis output and model results are filed in report storage 242.

The system creates the model results for SPICE in both lumped and distributed electrical circuit formats. It creates different SPICE decks for each of the specified frequencies. Besides creating SPICE decks, the system also provides the output 250 with summary files which provide the raw electrical parameter values; these files are created for each frequency of the analysis. Furthermore, output 250 comprises report files which contain information on the lumped values of the electrical parameters (for instance, for all leads of a leadframe) and a table that lists the variation of parameters over frequency.

Output 250 further comprises IBIS models which provide the electrical characteristics of the structure (for instance, of an electronic package) in the I/O Buffer Interface Specification format for use with electronic system design tools. In the S-parameter models, the system provides the scattering parameters of an electronic structure such as a leadframe.

The computer-implemented method of the invention uses control functions of the user interface 260 (see FIG. 2) in

a plurality of steps in the process flow. These process operations are controlled by automatically regulating execution and timing of the operations, as well as by responding to user commands. FIG. 6 summarizes these control functions schematically. The first operations control 610 is provided when segment data, filed in storage 224 and supplied by the sequence organizer, is read in sequence (process step 601). Based on this coordinated sequence, the electrical analysis calculation programs in the model data analysis 231 are run. The system instructs the start of the execution of each of these calculation programs.

In operations control II, designated 620 in FIG. 6, the system is processing signals at the end of each program execution in step 602. In process step 603, controlled by the third operations control 630, the system determines the successful completion of each calculation program. The system refuses failed program executions in process step 605 and reports the termination in step 606. The system accepts successful program executions and forwards them to decision point 604.

The question raised in process step 604 is whether the queue of segments is now empty or still contains one more segment to be forwarded to model data analysis. This search for the next segment is performed under process operations control IV (designated 640 in FIG. 6). If the answer is that there is still one more segment in queue, the sequence of process steps is repeated and operations control I (610) initiates in step 601 the reading of the next segment from segment data storage 224.

On the other hand, if the answer indicates that the queue of segments is empty, the system initiates, in controlled fashion, the storage of the completed analysis

results in the analysis output files 232. For this process step, operations control V (designated 650 in FIG. 6 and FIG. 5) instructs the advancement of the model results to the model data integrator.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

WE CLAIM:

1. A system for modeling an electronic structure, comprising:

an input data generator operable to generate input data comprising information describing a plurality of characteristics of a structure to be modeled, wherein said plurality of characteristics comprise a plurality of segments, subdivisions, and compositions;

a segmentation generator, coupled to said input data generator, operable to select segments of said structure to be modeled, to organize the sequence of said segments, to store the data related to said sequenced segments into a segment file, and to convert said segment file into a format suitable for electrical analysis;

an analysis generator, coupled to said segmentation generator, operable to electrically analyze said converted segment file in a plurality of calculation programs, executed in sequence, and to create electrical analysis output files;

an integrator, coupled to said analysis generator, operable to integrate said analysis output files in controlled sequence into a single model file and to store said file in a report storage; and

an output generator, coupled to said integrator, operable to create summary files in specific formats or displays.

2. The system according to Claim 1 wherein said segmentation generator comprises:

a segment selector, coupled to said input data

generator, operable to select segments and test lines of said structure to be modeled, select the input data correlated to said segments and test lines, and file said data in an input data storage;

a sequence organizer, coupled to said input data storage, operable to arrange said segments in the correct order for modeling and to create segment data files; and

a model data translator, coupled to said segment data file, operable to read said segment data files, to convert said segment into a format suitable for electrical analysis, and to create an analysis input storage, suitable for electrical analysis to be performed by a plurality of calculation programs executed in sequence.

3. The system according to Claim 2 further comprising a source of parametric data coupled to said sequence organizer.

4. The system according to Claim 1 wherein said electronic structure is an integrated circuit package.

5. The system according to Claim 1 wherein said electronic structure is a semiconductor device comprising an integrated circuit chip assembled in a package.

6. The system according to Claim 1 wherein said electronic structure is an electronic substrate comprising a conductive pattern embedded in an insulating medium.

7. The system according to Claim 1 wherein said electronic structure is a metallic leadframe used in electronic devices.

8. The system according to Claim 1 wherein said electronic structure is a semiconductor device assembled on an electronic substrate.

9. The system according to Claim 1 wherein said analysis generator comprises two-dimensional and three-dimensional electrical calculation means operable to cover all test lines and specified frequencies.

10. The system according to Claim 1 wherein said analysis generator produces a multitude of patterns comprising electrical resistances, capacitances, and inductances.

11. The system according to Claim 1 further comprising an integrator operable to calculate the scattering parameters for electrical high frequency assembly.

12. A computer system for modeling an electronic structure, comprising:

an input data generator operable to accept and store graphical, geometric, functional and compositional inputs and to create patterns of electrical conductors and insulators of the structure to be modeled;

a segment selector, coupled to said input data generator, operable to select segments and test lines of the structure to be modeled, to select the input data correlated to said segments and test lines from said data generator, and to create input data files;

a user interface including an operations controller, coupled to said input data files, operable to respond to user commands for controlling execution and timing of a multitude of operations of said computer system;

a sequence organizer, coupled to said input data file and further to additional parametric data storage, operable to arrange said segments in the correct order for modeling and to create segment data files;

a model data translator, coupled to said segment data file and further to said operations controller, operable to read said segment data files, to follow instructions from said operations controller, to convert said segment data into a format suitable for electrical analysis, and to store the results in an analysis input storage;

an analysis generator, coupled to said analysis input storage and further to said operations controller, operable to execute a plurality of electrical calculation programs in sequence and to create electrical analysis output files;

a model data integrator, coupled to said analysis output files and further to said operations controller, operable to integrate said analysis output files in controlled sequence into a single model file and to store said file in a report storage; and

an output generator, coupled to said model data integrator and further to said user interface, operable to create said model for each frequency analysis.

13. The computer system according to Claim 12 wherein said output generator creates said model in the format of SPICE-acceptable decks, summary and report files, IBIS decks, and displays.

14. The computer system according to Claim 12 further comprising a coupling of said parameter data storage to said user interface operable to transmit parametric data to said parameter data storage.

15. The computer system according to Claim 12 wherein said input data generator comprises:

an input unit operable to create patterns of

electrical conductors and insulators;

a graphical input unit operable to accept, select and read geometric and graphical programs; and

a parametric input unit operable to accept compositional and functional parameters.

16. The computer system according to Claim 15 wherein said geometric and graphical programs are selected from a group consisting of pro/ENGINEER and AutoCAD programs.

17. The computer system according to Claim 12 wherein said input data files, coupled to said segment selector, comprise storage of the input data after segment and test line selection in a format suitable for the selected graphical input program.

18. The computer system according to Claim 17 wherein said input data storage is in the IGES format for input data using Pro/ENGINEER graphics, and in the DXF format for input data using AutoCAD graphics.

19. The computer system according to Claim 12 wherein said operations controller is operable

to coordinate the sequence of electrical analysis calculation programs;

to instruct the start of the execution of each said calculation programs;

to process signals at the end of each program execution;

to control the successful completion of each said calculation programs, thereby providing acceptance of successful executions and refusal of failed executions;

to search for the next said segment in said sequence;

to control the storage of the completed analysis results in said analysis output files; and

to instruct their advancement to said model data integrator.

20. The computer system according to Claim 12 wherein said parametric data storage is operable to specify global parameters applicable to said electronic structure to be modeled.

21. The computer system according to Claim 12 wherein said analysis generator comprises electrical computational programs operable

for each electrical frequency;

for each test line of said structure to be modeled that needs two-dimensional analysis;

for each group of test lines of said structure to be modeled forming a three-dimensional segment;

for each test line of said structure to be modeled that needs mixed two-dimensional and three-dimensional analysis; and

for each test line of said structure to be modeled that traverses regions of different dielectric constants, electrical potentials, geometries, or symmetries.

22. A computer-implemented method for constructing a model of an electronic structure, comprising the steps of:

generating input data comprising information describing a plurality of characteristics of a structure to be modeled, wherein said plurality of characteristics comprise a plurality of segments, subdivision, and compositions;

generating segments of said structure to be modeled, selecting said segments, organizing the sequence of said segments, storing the data related to said sequenced segments into a segment file, and converting said segment file into a format

suitable for electrical analysis;

electrically analyzing said converted segment file in a plurality of calculation programs executed in sequence, and creating electrical analysis output files;

integrating said analysis output files in controlled sequence into a single model file and storing said file in a report storage; and

creating summary files in specific formats or displays.

23. The computer-implemented method according to Claim 22 wherein said step of generating input data of said electronic structure comprises:

creating patterns of electrical conductors and insulators of said electronic structure;

accepting, selecting and reading geometric and graphical programs describing a plurality of characteristics of said electronic structure; and

accepting compositional and functional parameters of said electronic structure.

24. The computer-implemented method according to Claim 22 wherein said step of generating segments comprises:

selecting segments and test lines of said structure to be modeled, selecting the input data correlated to said segments and test lines, and filing said data in an input data storage;

arranging said segments in the correct order for modeling, and creating a segment data storage; and

converting said segment data storage into a format suitable for electrical analysis, and creating an analysis input storage suitable for electrical analysis to be performed by a plurality of

programs executed in sequence.

25. The computer-implemented method according to Claim 24 wherein said step of converting said segment data storage into a format suitable for electrical analysis comprises:

reading the first segment from said segment data storage;

identifying all element groups that form a segment by a series of automatic steps comprising:

determining whether the end of the three-dimensional segment has been reached;

finding the edges of the geometry in said segment;

ordering said edges; and

determining whether the end of the two-dimensional segment has been reached;

converting the three-dimensional segment data and the two-dimensional segment data into the input format for electrical analysis;

transferring the data in said input format to the analysis input storage;

determining whether another segment is stored in said segment data storage; and

repeating all said steps until all segments in said segment data storage have been read and converted.

26. The computer-implemented method according to Claim 22 wherein said step of integrating said analysis output files into a single model file comprises:

reading the analysis output as stored in said analysis output files;

controlling said analysis output by reading each segment from said segment data storage and

collating a sequence list;

determining electrical connectivity as based on symmetry and branching of said collated sequence list;

creating analysis output in a suitable format; and

storing said analysis output in a report storage.

27. The computer-implemented method according to Claim 26 wherein said collated sequence list, based on symmetry and branching, generates a model of a complete electronic structure.

28. The computer-implemented method according to Claim 26 wherein said format of the analysis output is the SPICE-model format.

29. The computer-implemented method according to Claim 26 wherein said analysis output has lumped or distributed format.

30. The computer-implemented method according to Claim 22 further comprising the steps of :

controlling process operations by responding to user commands; and

automatically controlling execution and timing of a plurality of operations.

31. The computer-implemented method according to Claim 30 wherein said step of controlling operations comprises the steps of:

coordinating the sequence of the electrical analysis calculation programs;

instructing the start of the execution of each said calculation programs;

processing signals at the end of each program execution;

controlling the successful completion of each said calculation programs, thereby accepting

successful executions and refusing failed executions;

searching for the next said segment in said sequence;

controlling the storage of the completed analysis results in the analysis output files; and

instructing the advancement of said results to the model data integrator.

ABSTRACT

According to the electrical modeling system and method provided by the present invention, the electronic structure to be modeled is segmented into an ordered sequence of segments, each segment is electrically analyzed individually, and the resulting data is collated, or integrated back again whereby the model output is preferably created in a format generally suitable for electrical models of integrated circuits. Examples of electronic structures which can be modeled by the system and method of the invention include leadframes, packages, complete devices, and electronic devices assembled on motherboards.

FIG. 1

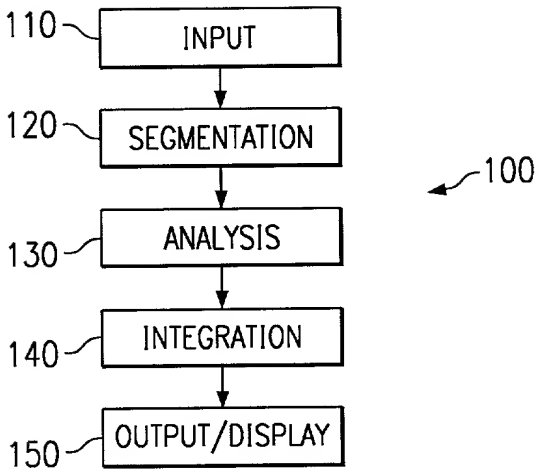
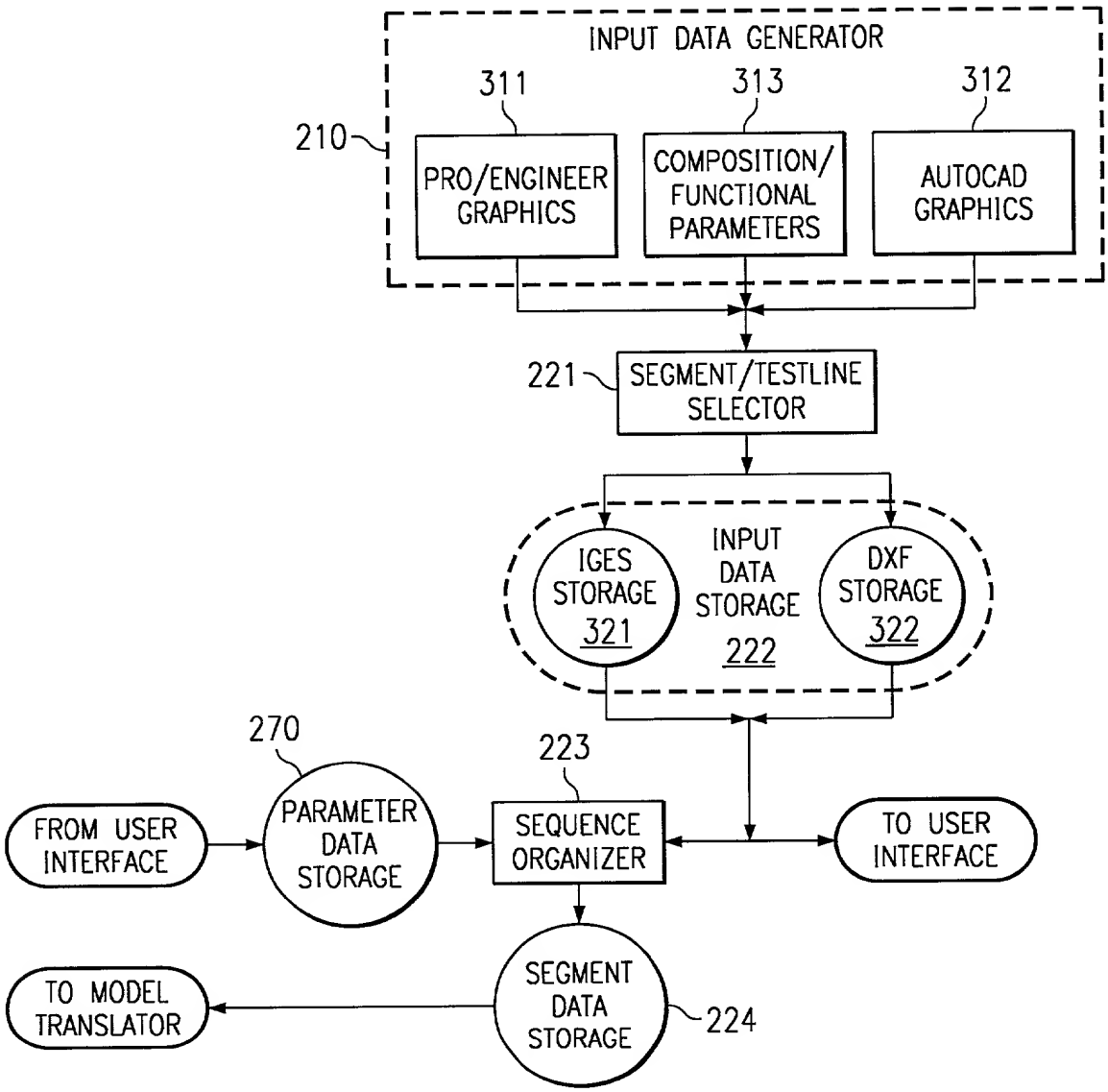

110
INPUT
120
SEGMENTATION
100
130
ANALYSIS
140
INTEGRATION
150
OUTPUT/DISPLAY

FIG. 3


INPUT DATA GENERATOR
311
313
312
210
PRO/ENGINEER GRAPHICS
COMPOSITION/ FUNCTIONAL PARAMETERS
AUTOCAD GRAPHICS
221
SEGMENT/TESTLINE SELECTOR
IGES STORAGE 321
INPUT DATA STORAGE 222
DXF STORAGE 322
270
223
FROM USER INTERFACE
PARAMETER DATA STORAGE
SEQUENCE ORGANIZER
TO USER INTERFACE
TO MODEL TRANSLATOR
SEGMENT DATA STORAGE
224

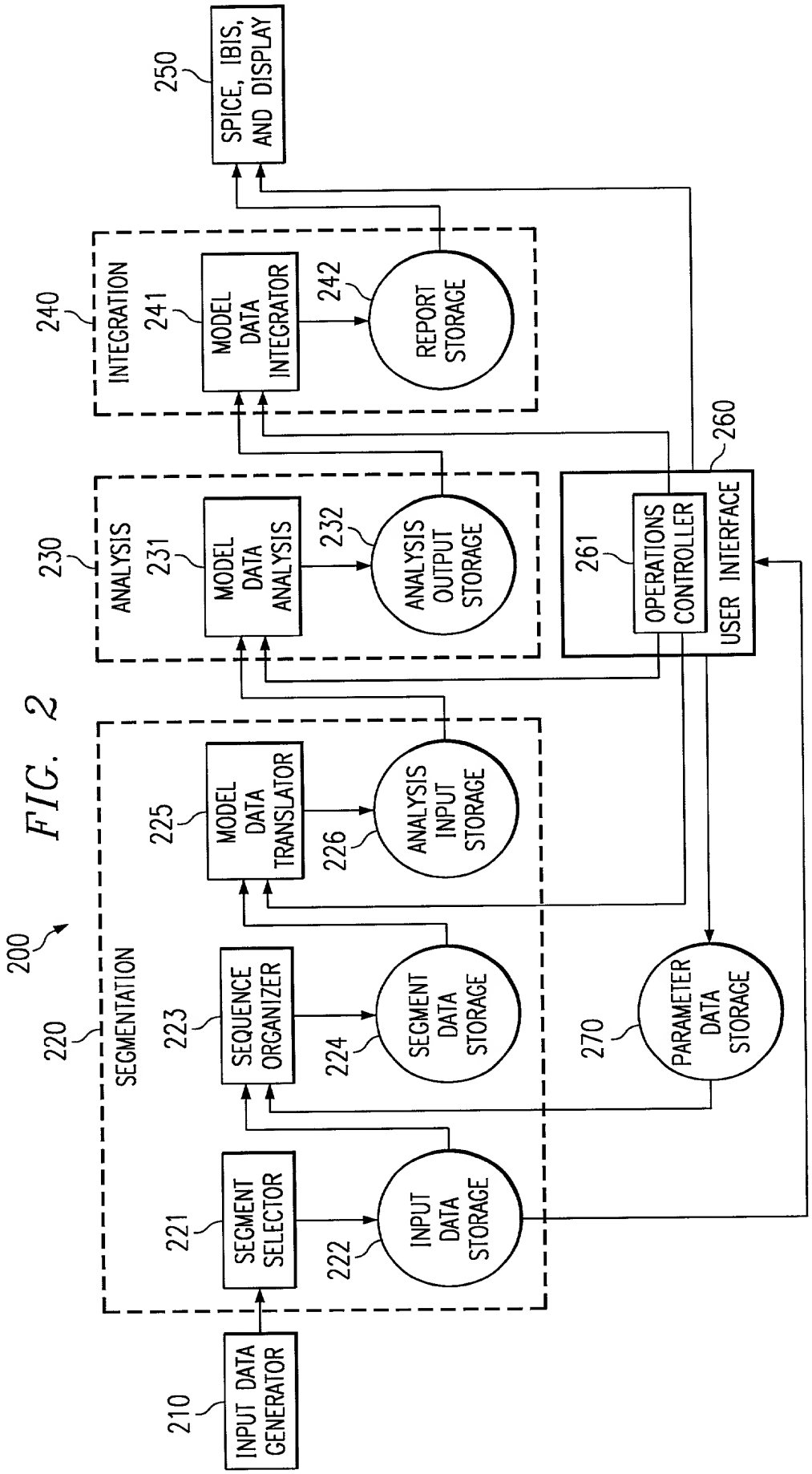

200
210
INPUT DATA GENERATOR
220
SEGMENTATION
221
SEGMENT SELECTOR
222
INPUT DATA STORAGE
223
SEQUENCE ORGANIZER
224
SEGMENT DATA STORAGE
225
MODEL DATA TRANSLATOR
226
ANALYSIS INPUT STORAGE
230
ANALYSIS
231
MODEL DATA ANALYSIS
232
ANALYSIS OUTPUT STORAGE
240
INTEGRATION
241
MODEL DATA INTEGRATOR
242
REPORT STORAGE
250
SPICE, IBIS, AND DISPLAY
260
USER INTERFACE
261
OPERATIONS CONTROLLER
270
PARAMETER DATA STORAGE

FIG. 2

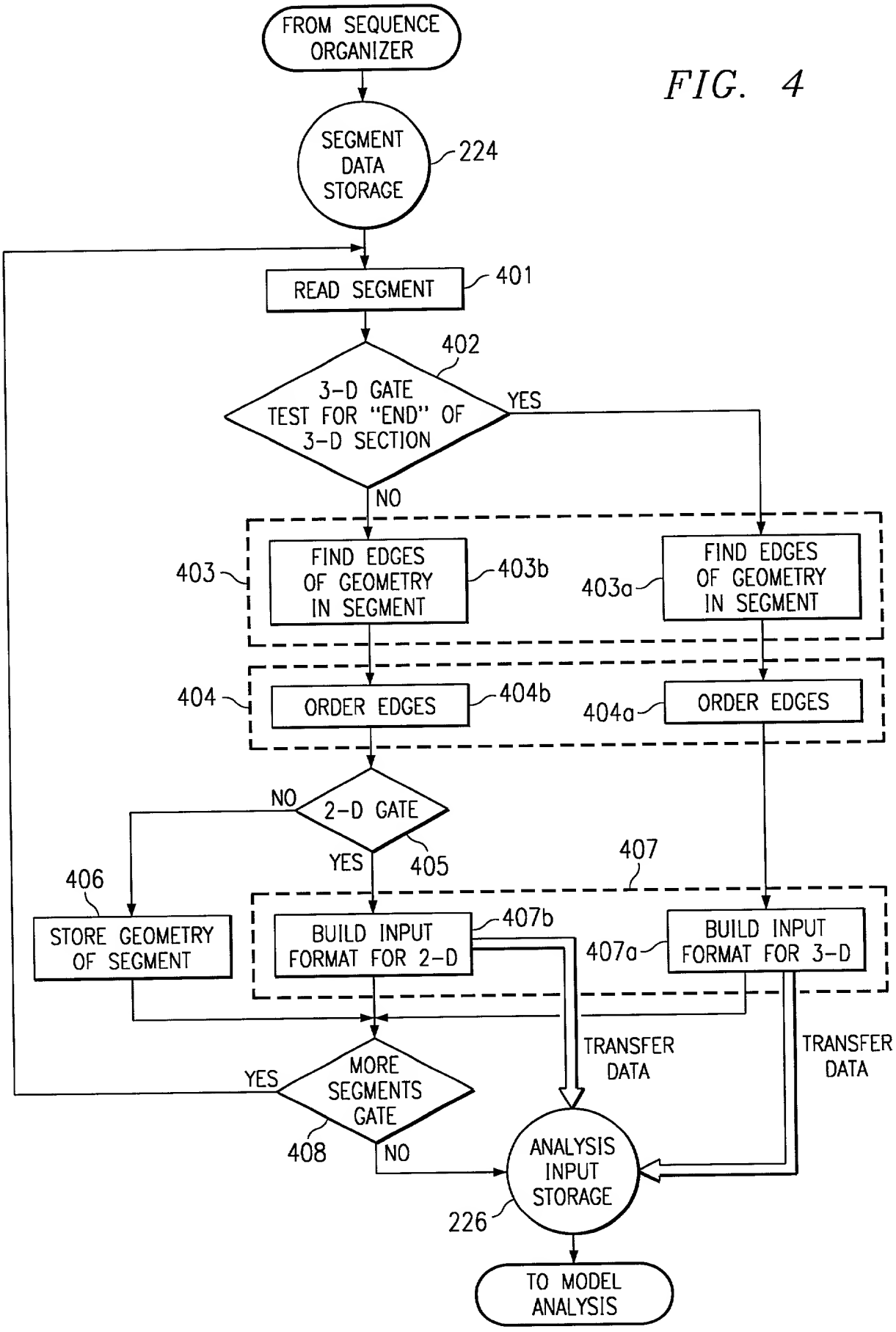

FROM SEQUENCE ORGANIZER
SEGMENT DATA STORAGE
224
READ SEGMENT
401
402
3-D GATE TEST FOR "END" OF 3-D SECTION
YES
NO
403
FIND EDGES OF GEOMETRY IN SEGMENT
403b
403a
FIND EDGES OF GEOMETRY IN SEGMENT
404
ORDER EDGES
404b
404a
ORDER EDGES
NO
2-D GATE
YES
405
407
406
STORE GEOMETRY OF SEGMENT
BUILD INPUT FORMAT FOR 2-D
407b
407a
BUILD INPUT FORMAT FOR 3-D
TRANSFER DATA
TRANSFER DATA
YES
MORE SEGMENTS GATE
408
NO
ANALYSIS INPUT STORAGE
226
TO MODEL ANALYSIS

FIG. 4

FIG. 5

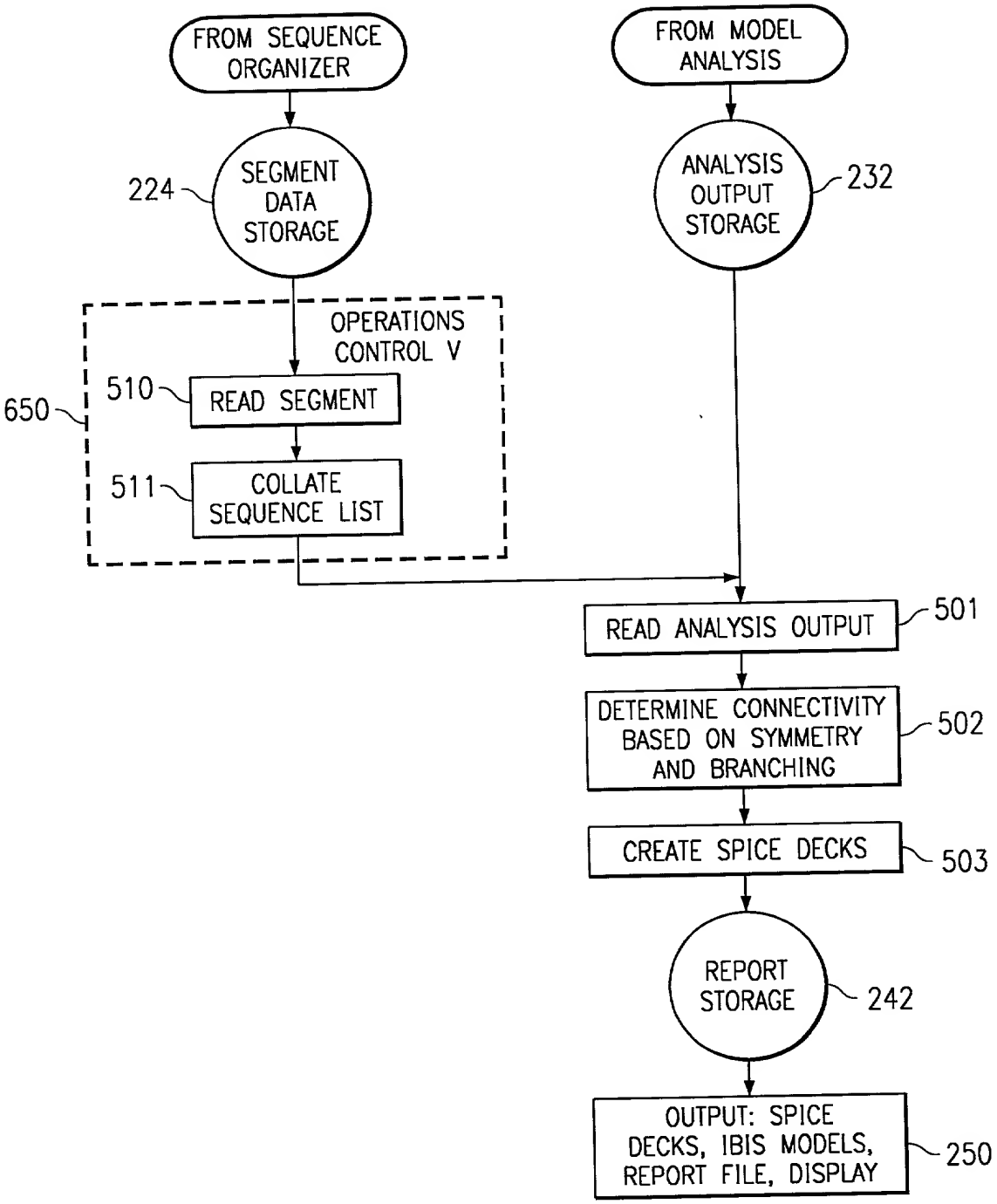
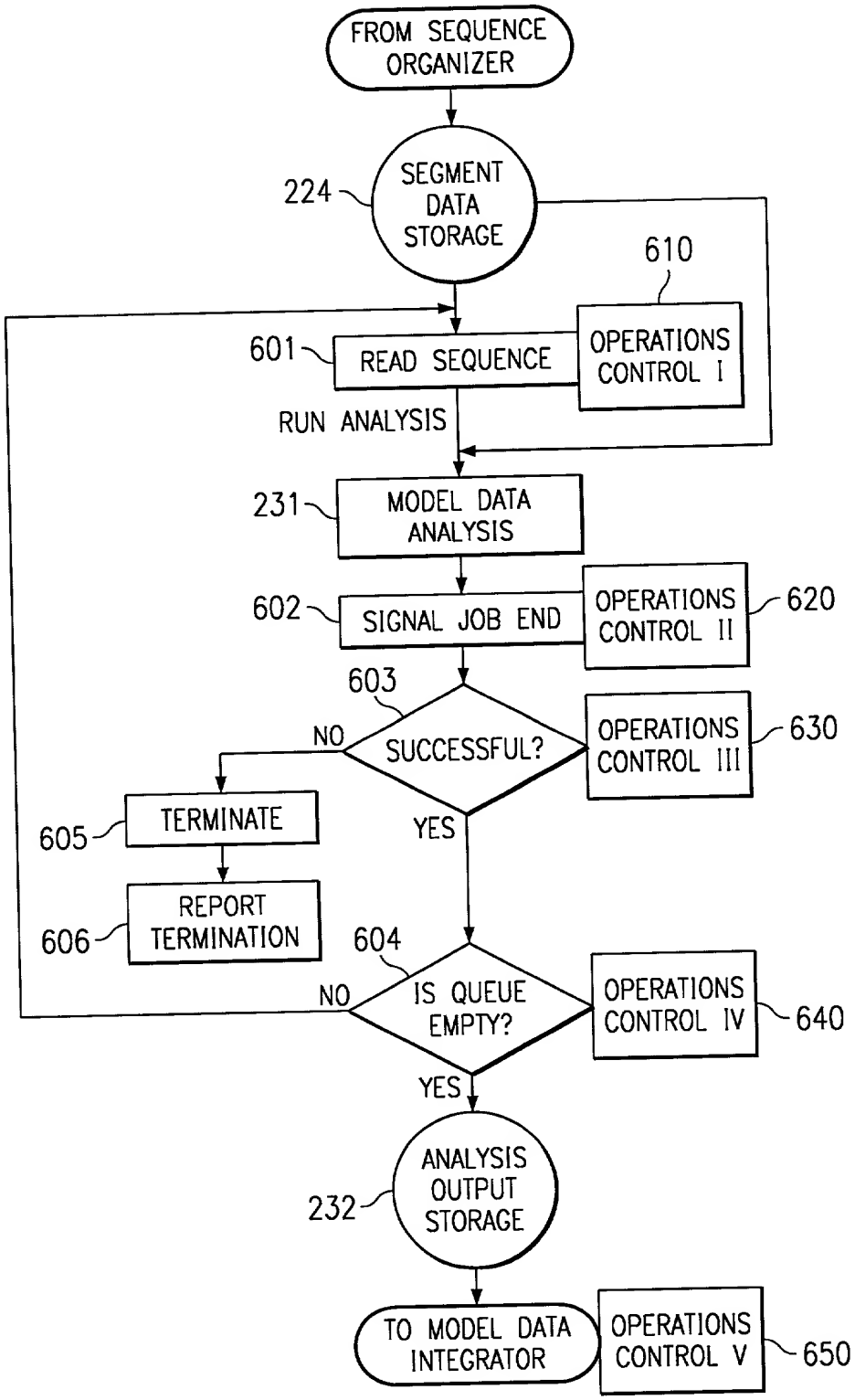

FROM SEQUENCE ORGANIZER
FROM MODEL ANALYSIS
224
SEGMENT DATA STORAGE
ANALYSIS OUTPUT STORAGE
232
OPERATIONS CONTROL V
650
510
READ SEGMENT
511
COLLATE SEQUENCE LIST
READ ANALYSIS OUTPUT
501
DETERMINE CONNECTIVITY BASED ON SYMMETRY AND BRANCHING
502
CREATE SPICE DECKS
503
REPORT STORAGE
242
OUTPUT: SPICE DECKS, IBIS MODELS, REPORT FILE, DISPLAY
250

FIG. 6


FROM SEQUENCE ORGANIZER
224
SEGMENT DATA STORAGE
610
601
READ SEQUENCE
OPERATIONS CONTROL I
RUN ANALYSIS
231
MODEL DATA ANALYSIS
602
SIGNAL JOB END
OPERATIONS CONTROL II
620
603
NO
SUCCESSFUL?
OPERATIONS CONTROL III
630
YES
605
TERMINATE
606
REPORT TERMINATION
604
NO
IS QUEUE EMPTY?
OPERATIONS CONTROL IV
640
YES
232
ANALYSIS OUTPUT STORAGE
TO MODEL DATA INTEGRATOR
OPERATIONS CONTROL V
650

ATTORNEY'S DOCKET NO.

TI-28063

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

System for Electrically Modeling an Electronic Structure, and Method of Operation

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

Richard L Donaldson, #25,673; Jay M. Cantor, #19,906; William B.Kempler, #28,228; Lawrence J.Bassuk, #29,043 and Gary C.Honeycutt, #20,250

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
Gary C. Honeycutt Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265	Gary C. Honeycutt (972) 238-7160

NAME OF INVENTOR: (1)	NAME OF INVENTOR: (2)	NAME OF INVENTOR: (3)
Michael A. Lamson	Subhendu Kundu	Ramani Ramesh
RESIDENCE & POST OFFICE ADDRESS: RR 2 Box 127E Anna, Texas 75409	RESIDENCE & POST OFFICE ADDRESS: #21 4B Cross, Atmananda Colony, SultanPalya, RT Nagar, Bangalore, Karnataka, India 560032	RESIDENCE & POST OFFICE ADDRESS: Flat-T1, Sarovara, 32, Papu Cottage Layout, Tata Silk Farm, Bangalore, Karnataka, India
COUNTRY OF CITIZENSHIP: United States	COUNTRY OF CITIZENSHIP: India	COUNTRY OF CITIZENSHIP: India
SIGNATURE OF INVENTOR: X Michael A. Lamson	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: X January 29, 1999	DATE:	DATE:

ATTORNEY'S DOCKET NO.
TI-28063

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: System for Electrically Modeling an Electronic Structure, and Method of Operation		
POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH Richard L. Donaldson, #25,673; Jay M. Cantor, #19,906; William B.Kempler, #28,228; Lawrence J.Bassuk, #29,043 and Gary C.Honeycutt, #20,250		
SEND CORRESPONDENCE TO: Gary C. Honeycutt Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265		DIRECT TELEPHONE CALLS TO: Gary C. Honeycutt (972) 238-7160
NAME OF INVENTOR: (1) Michael A. Lamson	NAME OF INVENTOR: (2) Subhendu Kundu	NAME OF INVENTOR: (3) Ramani Ramesh
RESIDENCE & POST OFFICE ADDRESS: RR 2 Box 127E Anna, Texas 75409	RESIDENCE & POST OFFICE ADDRESS: #21 4B Cross, Atmananda Colony, SultanPalya, RT Nagar, Bangalore, Karnataka, India 560032	RESIDENCE & POST OFFICE ADDRESS: Flat-T1, Sarovara, 32, Papu Cottage Layout, Tata Silk Farm, Bangalore, Karnataka, India
COUNTRY OF CITIZENSHIP: United States	COUNTRY OF CITIZENSHIP: India	COUNTRY OF CITIZENSHIP: India
SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR: X S. Kundu	SIGNATURE OF INVENTOR: X Ramani
DATE:	DATE: X 27 Jan 1999	DATE: X 27 Jan 1999